

MECHANICAL PROCESSING OF SILICON SUBSTRATE, SURFACE CLEANING WITH ABRASIVE MATERIALS

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Abstract

This paper explores the processing of silicon substrates in microelectronics, specifically mechanical processing, polishing, oxidation, and other treatments, as well as the theoretical modeling of the thermoelectric properties of porous SiNWs.

Keywords: Semiconductor devices, integrated circuits, local diffusion, thermoelectric properties of porous SiNWs, silicon substrate, silicon oxide, doping, polishing, oxidation, photolithography, p-n junctions.

Introduction

Integrated circuits are primarily made from single-crystal silicon due to the high quality of the SiO₂ layer, which can be produced through a relatively simple process. The technology for obtaining large-diameter silicon single crystals is relatively inexpensive and well established. A wafer cut from a silicon single crystal, subjected to certain mechanical and chemical treatments, is referred to as the substrate for integrated circuits[1].

Diamond powder-coated metal discs are used for cutting wafers from silicon ingots. The thickness of the disc is 0.1-0.15 mm (Figure 1). The feed rate of the silicon ingot holder in the cutting equipment is 20-30 mm/min. Due to the impact of abrasive material (powder) on the surface of the cut wafer, a damaged layer of the monocrystalline structure is formed. This layer has a thickness of 10-30 μm, corresponding to cleanliness of class 7-8. To create an integrated circuit, the surface roughness of the wafer should not exceed 0.02-0.1 μm. This is even higher than the cleanliness of class 14. To achieve such smoothness, wafers are polished (grinding) and then buffed (polishing) using special high-precision equipment with microminerals.



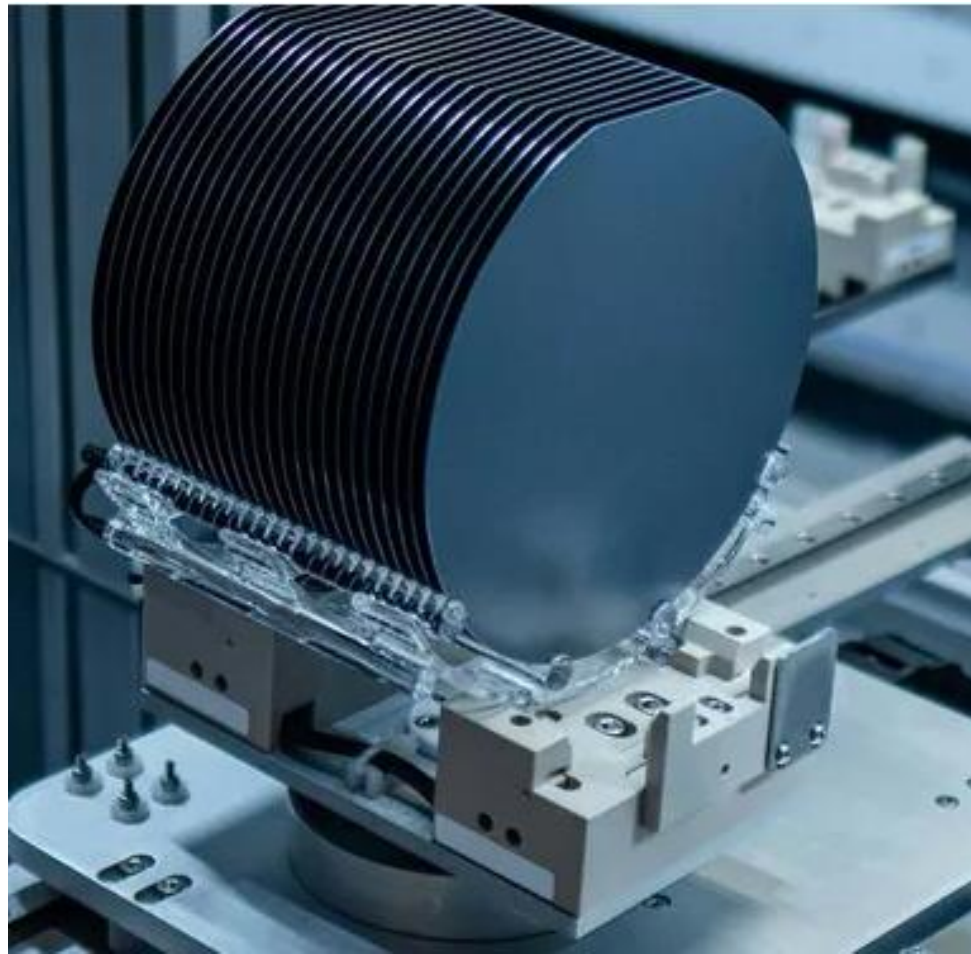


Figure 1. Silicon

A glass grinding tool (grinder) is used when grinding with M14-M15 grade microminerals. The surface is polished using diamond paste, resulting in a lattice-like finish [2.3].

LITERATURE REVIEW AND METHODOLOGY

Both sides of the wafer are polished. Polishing is only performed on the surface that will form the integrated circuit. In M14-grade microminerals, the powder particle size ranges from 14 to 10 μm , while in M10-grade microminerals, the powder size is between 10 and 7 μm . ASM-3/2 synthetic diamond powder, with a particle size distribution of 3/2, has large particles of 3 μm and fine particles of 2 μm .

Table 1

Surface cleanliness class of the wafer

mikro-kukun	Broken Layer Thickness, μm	Surface Cleanliness Class of the Wafer
M 14	20-30	7
M10	15-25	8-9
ASM 3/2	9-11	12-13
ASM 1/0.5	5-7	13
ASM 0.5/0.3	3-dan kichik	13-14
ASM 0.3/0.1	1-dan kichik	14

After polishing and buffing, the wafer surface is cleaned of micro-dust residues and technical stains. This is done through chemical cleaning using solvents and acids. The second method is a physical cleaning method, where contaminants bound to the silicon molecules are removed by heating or ion bombardment, providing high energy to eject the impurities. Powder residues are cleaned using ultrasonic equipment with solvents such as trichloroethylene, toluene, and carbon tetrachloride. To remove organic substances from the molecules, the wafer is boiled in sulfuric acid (H₂SO₄). To remove metal atoms, it is boiled in HCl and HNO₃ and washed in HF. The wafer is always washed at the end of the process in deionized (DI) water to remove ions. One of the methods for checking the cleanliness of the wafer surface is to observe the polished surface under a microscope. Light is incident on the wafer surface at a very small angle. The contaminated areas appear dark, while the scattered light from the impurities appears bright under the microscope. Another method is to check the surface when wet: if there are oils present, the water will not form a uniform layer but will break into droplets.

Various types of water are used in the wafer cleaning process:

Distilled water, with specific resistance $p=200\text{k}\Omega/\text{cm}$. Tap water is boiled and then re-condensed.

Bidistilled water, with specific resistance $p=500\text{ k}\Omega/\text{cm}$. Distilled water is boiled and then re-condensed.

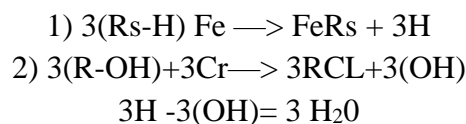
RESULTS:

Deionized (ion-free) water has a specific resistance of $p=20\text{m}\Omega/\text{cm}$ (see Figure 2). Distilled water is obtained by passing it through ion-exchange resins. These resins are of two types:

1. **Cations** (which absorb metal ions),
2. **Anions** (which absorb ions from acidic residues).

The chemical formula for cations is: R-H; for anions: R-OH.

For example, the cleaning process for **FeCl₃** occurs as follows:



(1) The Fe ion in (1) binds with R and forms an H ion.

(2) The Cl ion in (2) binds with R and forms an OIT ion. The F and OIT ions bind together, and water is formed

Explanation; Ion exchange method: In this method, distilled water is passed through ion-exchange resins. These resins are of two types:

- o **Cations** (which absorb metal ions),
- o **Anions** (which absorb acid residues and other anions).

For example, in the case of **FeCl₃** being cleaned, the Fe₃ion reacts with the cations, and the Cr₃ion reacts with the anions. As a result, **H⁺** and **OH⁻** ions are produced, which combine to form water.

This process is used to remove contaminants and ions from the surface of wafers or semiconductor materials.



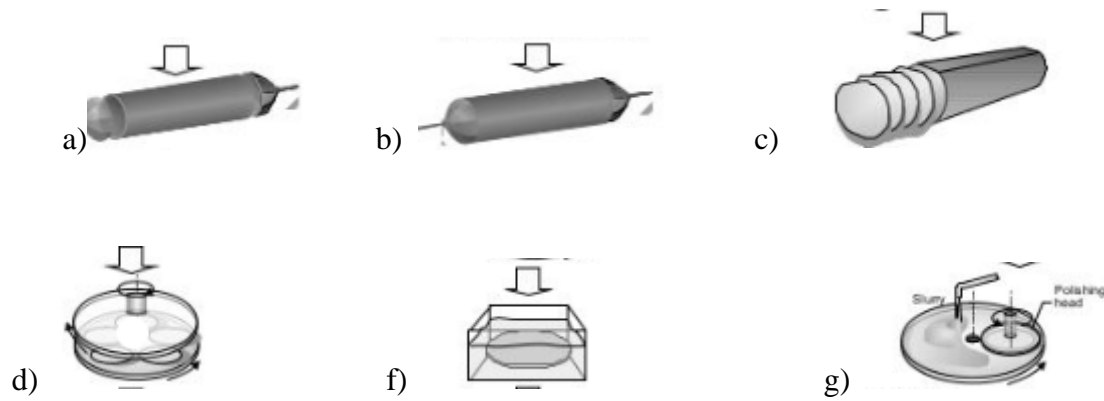


Figure 2. a-c, Diamond powder is applied to metallic disks to cut the wafer from silicon ingots; d-g, The wafer is processed using abrasive material and cleaned with ion-exchanged water, which is obtained by distilling natural tap water and then deionizing it. The specific resistance is $p=1M\Omega/cm$ at $200^{\circ}C$.

“B” Mark Ion-exchanged Water is further deionized from "V" mark deionized water, then filtered through inert materials with pore sizes of 10 micrometers to remove insoluble particles. The specific resistance is $p=10M\Omega/cm$.

“A” Mark Ion-exchanged Water is filtered through special filter materials with pore sizes of 0.5 micrometers, obtained from "B" mark deionized water. The specific resistance in this case is $p=20M\Omega/cm$.

The word “**abrasive**” comes from the Latin word for “to scrape” or “to wear away” The main property of abrasive materials is their hardness. The hardest material is diamond, which corresponds to a grade of 10 on the Mohs scale, followed by corundum at grade 9, topaz at grade 8, and quartz at grade 7.

The abrasive ability of materials is evaluated based on the amount of material removed from the surface of the material being worked on, per unit of time, using an abrasive material. If diamond's abrasive ability is taken as 1, then carbide's abrasive ability is 0.6, silicon carbide's is 0.5, monocorundum's is 0.25, and electrocorundum's is 0.15.

In semiconductor and integrated circuit manufacturing, the following abrasive materials are used:

Diamond: Artificial diamonds produced under high pressure and temperature from graphite are used in industry.

Silicon carbide: A chemical compound of silicon and carbon. The color of silicon carbide can range from green to black, depending on the level of chemical purity. Its pure form is colorless, while impurities can make it green or black. Black silicon carbide has lower strength.

Boron carbide: A chemical compound of boron and carbon.

Electrocorundum: Crystalline aluminum oxide (Al_2O_3), a white substance. Three types of electrocorundum are produced:

- White: 98.5–99.5% Al_2O_3 content.
- Normal electrocorundum: 91–96% Al_2O_3 content.



- Black electrocorundum: 65–75% Al_2O_3 content.

Chromium oxide: A green powder.

Aerosil: A porous bluish-white powder, consisting of pure silicon dioxide. The following grades are produced: A-175, A-300, A-380, with average particle sizes ranging from 10-40, 5-20, and 5-15 micrometers, respectively.

Various porous SiNWs (Silicon Nanowires) have temperature-dependent effective thermal conductivity k_{eff} , effective electrical conductivity and Seebeck coefficient S . The first number refers to the porosity of SiNWs, the middle number represents the concentration of boron doping measured by secondary ion mass spectrometry (SIMS), and the last number refers to the SiNW diameter. Note that k_{eff} are not normalized by porosity but are based on the nanowire diameter. For three samples with $d_s=46\%$ and $p=2.2 \times 10^{20} \text{ cm}^{-3}$ (152, 171, and 184 nm), the calculated thermoelectric performance (ZT values) is compared with previously measured ZT results for a single coarse SiNW, thin SiNW array, polycrystalline Si nanotube networks, hole-doped Si nanobulk, and bulk Si (8.1×10^{-6} doped) (see Figure 3). Error bars represent the uncertainties in the ZT calculation due to measurement errors in k , σ and S .

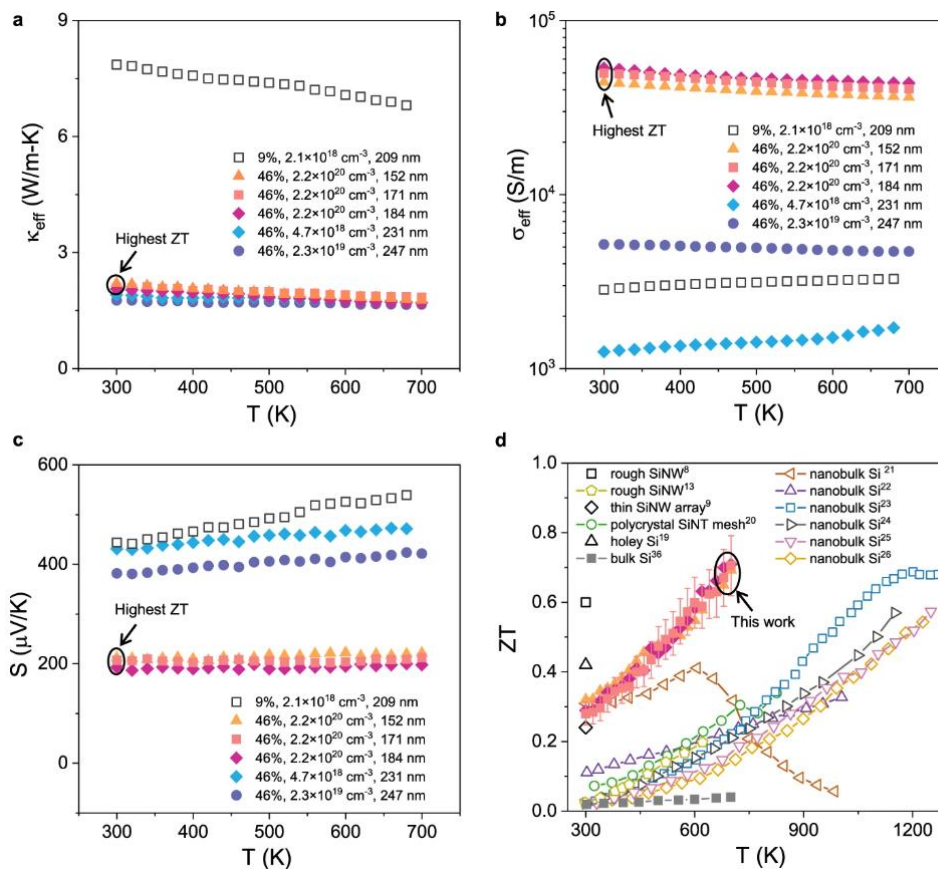


Figure 3. Theoretical Modeling of Thermoelectric Properties of Porous SiNWs

To eliminate the effect of temperature variation from the temperature controller and enhance sensitivity for measuring thermal conductivity, a Wheatstone bridge circuit was adopted by introducing a void device on the sensitive side of the measuring device. During thermal measurements, the Seebeck coefficient for each sample was measured by simultaneously tracking the temperature difference across the heating and sensing membranes, as well as the



induced voltage difference across the two internal electrodes of the measuring device (SR560) [4,9,10].

Discussion

Processes such as mechanical processing, polishing, and oxidation can significantly alter the surface structure and physical properties (e.g., hardness, elasticity, thermal conductivity) of silicon nanowires (SiNWs). This, in turn, affects the thermoelectric properties, specifically the relationship between thermal and electrical conductivity. In the field of microelectronics, various treatments applied to silicon substrates—particularly mechanical processing, polishing, oxidation, and other processes—have been studied for their effects on the thermoelectric properties of “porous silicon nanowire” (SiNW) structures. The main goal of the research was to analyze and theoretically model how the thermoelectric properties of silicon materials change with mechanical and chemical treatments.

Conclusion

Through theoretical modeling, ideal treatment conditions and methods for optimizing the thermoelectric efficiency of silicon nanostructures were defined. The study also deeply analyzed various factors related to the thermal and electrical properties of porous SiNWs, as well as their thermoelectric efficiency. These factors include crystal structure, porosity (porous structure), external influences, and the interactions between these elements.

As a result, processing techniques for silicon-based porous nanowires can significantly improve their thermoelectric properties, thereby expanding their potential applications in microelectronics and thermoelectric devices. This research also provides a solid scientific foundation for developing new approaches and strategies for the design and production of silicon-based thermoelectric materials in the future [3,5].

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